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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
BUR920040136US1

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Application Number	Filed
10/709,811	05/28/2004

First Named Inventor: Austin, *et al.*

Art Unit	Examiner
2817	Chang, Joseph

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

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The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☑ attorney or agent of record.
Registration number 47,820

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

Khoi Le Nguyen
Signature

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April 18, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.
Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

GROUNDS OF REJECTION AND ARGUMENTS

GROUND OF REJECTION 1

Claims 9-12, 14,-15, and 17-20 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Schorn et al. (US 6,278,334).

Claim 9:

Appellants respectfully contend that Schorn does not anticipate claim 9, because Schorn does not not teach "(b) a control circuit including a first switch circuit and a first resistance adjusting circuit electrically coupled in series between the output node and the **first operating voltage**" of claim 9 (bold emphasis added).

More specifically, in page 2 of the final Office Action (dated January 24, 2006), the Examiner indicates that the first operating voltage is VDD and that the "control circuit including a first switch circuit (upper transistor of 46) and a first resistance adjusting circuit (lower transistor of 46)" of FIG. 4 of Schorn anticipates the control circuit of claim 9. However, this control circuit 46 of Schorn is coupled between the output node and the **second operating voltage** (Ground). In contrast, the control circuit of claim 9 is coupled between the output node and the **first operating voltage**.

In addition, as a second argument by Appellants, Schorn does not teach "the first resistance adjusting circuit electrically couples the first switch circuit to the output node" of claim 9. More specifically, FIG. 4 of Schorn shows that the first switch circuit (upper transistor of 46) electrically couples the first resistance adjusting circuit (lower transistor of 46) to the output node OUT. In contrast, claim 9 claims that the first resistance adjusting circuit electrically couples the first switch circuit to the output node (i.e., the other way around).

In page 2 of the final Office Action, the Examiner argues that "...every element and connection are the same as the one in this application and therefore any functional limitations recited in the claims are inherently present." In response, Appellants would like to note that the first and second arguments by Appellants above show that the control circuit 46 of Schorn (FIG. 4) and the control circuit of claim 9 are not structurally the same. Therefore, the Examiner's conclusion that "therefore any functional limitations recited in the claims are inherently present" is not persuasive. For instance, with reference to FIG. 4 of Schorn, in response to the input signal (IN) decreasing in voltage towards the second operating voltage (ground), the resistance of the first switch circuit (upper transistor of 46) is **increased** (the operating principle of an n-channel transistor). In contrast, in claim 9, "in response to the input signal decreasing in voltage towards the second operating voltage, the first switch circuit is configured to **decrease** in resistance" (bold emphasis added).

Based on the preceding arguments, Appellants respectfully maintain that Schorn does not anticipate claim 9, and that claim 9 is in condition for allowance.

Claim 10:

Since claim 10 depends from claim 9, Appellants contend that claim 10 is likewise in condition for allowance.

Claim 11:

Since claim 11 depends from claim 10, which is in condition for allowance as argued above, Appellants contend that claim 11 is likewise in condition for allowance.

Claim 12:

Since claim 12 depends from claim 9, which is in condition for allowance as argued above, Appellants contend that claim 12 is likewise in condition for allowance.

Claim 14:

Since claim 14 depends from claim 9, which is in condition for allowance as argued above, Appellants contend that claim 14 is likewise in condition for allowance.

Moreover, Schorn does not teach "The oscillator delay stage circuit of claim 9, wherein the inverting circuit comprises a **CMOS inverter**" of claim 14 (bold emphasis added). More specifically, Schorn, from FIG. 2 to FIG. 4, only teaches that the oscillator delay stage circuit comprises the inverting circuit 16 (FIG. 2) or the inverting circuit 44 (FIG. 4) without saying further detail about these inverting circuits 16 and 44. In contrast, in claim 14, the inverting circuit is a CMOS inverter.

In page 3 of the final Office Action, the Examiner argued that "Although Schorn does not explicitly disclose that the inverter 44 is CMOS, one of ordinary skill in the art would have recognized that the inverter 44 is of CMOS because CMOS inverters are well known in the art". In response, Appellants agree that CMOS inverters are well known in the art. However, it's not inherent that the inverter 44 in FIG. 4 of Schorn is a CMOS inverter (it can be any other inverters, for example an inverter can comprise only one n-channel transistor). The Examiner also argued that "Figures 1-3 shows CMOS inverters". In response, Appellants note that, contrary to the Examiner's belief, the entire Schorn patent does not mention any CMOS inverter.

Based on the preceding arguments, Appellants respectfully maintain that Schorn does not anticipate claim 14, and that claim 14 is in condition for allowance.

Claim 17:

Appellants respectfully contend that Schorn does not anticipate claim 17, because Schorn does not teach "a control circuit including a switch circuit and a resistance adjusting circuit electrically coupled in series between the output node and the **first operating voltage**" of claim 17 (bold emphasis added).

More specifically, in page 2 of the final Office Action, the Examiner indicates that the "control circuit including a first switch circuit (upper transistor of 46) and a first resistance adjusting circuit (lower transistor of 46)" of FIG. 4 of Schorn anticipates the control circuit of claim 9. However, this control circuit 46 of Schorn is coupled between the output node and the **second operating voltage**. In contrast, the control circuit of claim 17 is coupled between the output node and the **first operating voltage**.

In page 2 of the final Office Action, the Examiner argues that "...every element and connection are the same as the one in this application and therefore any functional limitations recited in the claims are inherently present." In response, Appellants would like to note that the

argument by Appellants above show that the control circuit 46 of Schorn (FIG. 4) and the control circuit of claim 17 are not structurally the same. Therefore, the Examiner's conclusion that "therefore any functional limitations recited in the claims are inherently present" is not persuasive. For instance, with reference to FIG. 4 of Schorn, in response to the input signal (IN) decreasing in voltage towards the second operating voltage (ground), the resistance of the first switch circuit (upper transistor of 46) is **increased** (the operating principle of an n-channel transistor). In contrast, in claim 17, "(c) in response to an input signal decreasing in voltage at the input node...(ii) **decreasing** the resistance of the switch circuit" (bold emphasis added).

Based on the preceding arguments, Appellants respectfully maintain that Schorn does not anticipate claim 17, and that claim 17 is in condition for allowance.

Claim 18:

Since claim 18 depends from claim 17, which is in condition for allowance as argued above, Appellants contend that claim 18 is likewise in condition for allowance.

Moreover, Schorn does not teach "the resistance adjusting circuit electrically couples the switch circuit to the output node" of claim 18. More specifically, FIG. 4 of Schorn shows that the switch circuit (upper transistor of 46) electrically couples the resistance adjusting circuit (lower transistor of 46) to the output node OUT. In contrast, claim 18 claims that the resistance adjusting circuit electrically couples the switch circuit to the output node (i.e., the other way around).

Based on the preceding arguments, Appellants respectfully maintain that Schorn does not anticipate claim 18, and that claim 18 is in condition for allowance.

Claim 19:

Since claim 19 depends from claim 17, which is in condition for allowance as argued above, Appellants contend that claim 19 is likewise in condition for allowance.

Claim 20:

Since claim 20 depends from claim 17, which is in condition for allowance as argued above, Appellants contend that claim 20 is likewise in condition for allowance.

Moreover, Schorn does not teach "The method of claim 17, wherein the inverting circuit comprises a **CMOS inverter**" of claim 14 (bold emphasis added). More specifically, Schorn, from FIG. 2 to FIG. 4, only teaches that the oscillator delay stage circuit comprises the inverting circuit 16 (FIG. 2) or the inverting circuit 44 (FIG. 4) without saying further detail about these inverting circuits 16 and 44. In contrast, in claim 20, the inverting circuit is a CMOS inverter.

In page 3 of the final Office Action, the Examiner argued that "Although Schorn does not explicitly disclose that the inverter 44 is CMOS, one of ordinary skill in the art would have recognized that the inverter 44 is of CMOS because CMOS inverters are well known in the art". In response, Appellants agree that CMOS inverters are well known in the art. However, it's not inherent that the inverter 44 in FIG. 4 of Schorn is a CMOS inverter (it can be any other inverters, for example an inverter can comprise only one n- channel transistor). The Examiner also argued that "Figures 1-3 shows CMOS inverters". In response, Appellants note that, contrary to the Examiner's belief, the entire Schorn patent does not mention any CMOS inverter.

Based on the preceding arguments, Appellants respectfully maintain that Schorn does not anticipate claim 20, and that claim 20 is in condition for allowance.

GROUND OF REJECTION 2

Claims 6, 15, and 17 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Schorn et al. (US 6,278,334) in view of Abe et al. (US 6,271,730).

Claim 6:

Regarding claim 6, claim 6 is now rewritten in a dependent form of claim 1 with the limitations of the original claim 6. Since claim 6 depends from claim 1, which is allowed as indicated in the final Office Action, Appellants contend that claim 6 is likewise in condition for allowance.

Claim 15:

Since claim 15 depends from claim 9, which is in condition for allowance as argued above, Appellants contend that claim 15 is likewise in condition for allowance.

Claim 17:

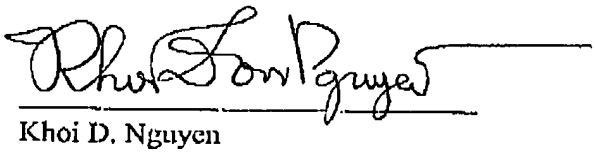
Regarding claim 17, in page 3 of the final Office Action, the Examiner argued that "Although Schorn does not explicitly disclose that the inverter 44 is CMOS, one of ordinary skill in the art would have recognized that the inverter 44 is of CMOS because CMOS inverters are well known in the art, as an example, Figures 1-3 shows CMOS inverters". In response, Appellants note that, there is no feature "the inverting circuit comprises a CMOS inverter" in claim 17.

Based on the preceding arguments, Appellants respectfully maintain that claim 17 is not unpatentable over Schorn in view of Abe, and that claim 17 is in condition for allowance.

SUMMARY

In summary, Appellants respectfully request reversal of the January 24, 2006 Office Action rejection of claims 9-12, 14,-15, and 17-20.

Respectfully submitted,



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